CLAIMS

1. A semiconductor packaging structure for computed tomography, the semiconductor packaging structure comprising an array of photodiodes extending in two dimensions and a connector interface, said array of photodiodes comprising: a plurality of anodes at first surfaces of a corresponding plurality of substrates divided from a single substrate; a corresponding plurality of cathodes at second surfaces of the plurality of substrates; and an electrical interconnection between the plurality of anodes; said connector interface comprising a corresponding plurality of contacts, electrically connected to the respective cathodes, for reading a corresponding plurality of output signals provided by the plurality of cathodes, said plurality of substrates being provided on the connector interface.

2. A semiconductor packaging structure according to claim 1 wherein a passivation layer connects the plurality of substrates.

3. A semiconductor packaging structure according to claim 1 or 2 wherein the plurality of cathodes comprise a plurality of conductive layers at the surface of the plurality of substrates.

4. A semiconductor packaging structure according to claim 3, wherein there is further provided a metal layer on each conductive layer.

5. A semiconductor packaging structure according to any one of claims 1 to 4 wherein the plurality of anodes comprise a plurality of active regions formed at the first surface.

6. A semiconductor packaging structure according to claim 5 wherein there is further provided a metal contact for each active region.

7. A semiconductor packaging structure according to any one of claims 1 to 6 wherein the electrical interconnection is provided by wire bonding.

8. A semiconductor packaging structure according to any one of claims 1 to 6 wherein the electrical interconnection is provided by metal contacts.

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9. A semiconductor packaging structure according to any one of claims 1 to 6 wherein the electrical interconnection is provided by a conductive sheet.

10. A semiconductor packaging structure according to any one of claims 1 to 9 wherein the plurality of contacts are connected to the plurality of cathodes by an epoxy.

11. A semiconductor packaging structure according to any one of claims 1 to 10 wherein the connector interface provides a contact for the anodes.

12. An imaging system including at least one semiconductor packaging structure according to any one of claims 1 to 11.

13. A computed tomography imaging system including at least one semiconductor packaging structure according to any one of claims 1 to 11.

14. A radiation detector including a plurality of semiconductor packaging structures according to any one of claims 1 to 11, wherein the plurality of said semiconductor packaging structures are placed adjacent to each other in a matrix to form a photo-detector array.

15. A radiation detector according to claim 14 wherein the matrix extends in two directions.

16. An imaging system comprising: a radiation detector according to claim 14 or claim 15, a radiation source facing the radiation detector, and means for controlling the radiation detector and the radiation source.

17. An imaging system according to claim 16 wherein the radiation source is an X-ray tube equipped with a high-voltage generator.

18. An imaging system according to claim 16 or claim 17 wherein the radiation detector and the radiation source are radially mounted in a cylindrical scanning structure.

19. An imaging system according to any one of claims 16 to 18 wherein the means for controlling comprises a computer system.

20. A method of forming a semiconductor packaging structure for computed tomography, said semiconductor packaging structure including an array of photodiodes extending in two dimensions and a connector interface providing a

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plurality of contacts for reading output signals of the array, said method comprising: forming a plurality of anodes at a first surface of a substrate; forming a corresponding plurality of cathodes at a second surface of the substrate; dividing the substrate to a corresponding plurality of substrates; electrically interconnecting the plurality of anodes; and electrically connecting the plurality of contacts to the respective cathodes, wherein said plurality of substrates are provided on the connector interface and the plurality of cathodes provide the plurality of output signals of the array.

21. A method according to claim 20 wherein the step of forming a plurality of cathodes comprises providing a plurality of conductive layers on the second surface of the substrate.

22. A method according to claim 20 or 21 wherein the plurality of conductive layers are formed by providing a continuous conductive layer on the second surface of the substrate, and electrically isolating portions of the continuous layer to form the plurality of conductive layers.

23. A method according to claim 22 wherein the portions of the conductive layer are electrically isolated by etching or cutting the continuous conductive layer.

24. A method according to claim 23 wherein the step of etching or cutting further etches the substrate.

25. A method according to claim 24 wherein the substrate is etched or cut completely.

26. A method according to claim 24 wherein a passivation layer on the first surface of the substrate is unaffected by the cut or etch.

27. A method according to claim 25 or 26 wherein there is thus formed a plurality of electrically isolated substrate portions.

28. A method according to any one of claims 23 to 27 wherein the etch or cut is patterned such that a contiguous area is etched or cut around each cathode.

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29. A method according to any one of claims 20 to 28 wherein the step of interconnecting the plurality of anodes includes forming wire bonding between anodes on the first surface of the substrate.

30. A method according to any one of claims 20 to 28 wherein the step of interconnecting the plurality of anodes includes providing a metal interconnect between anodes on the first surface of the substrate.

31. A method according to any one of claims 20 to 28 wherein the step of interconnecting the plurality of anodes includes providing a conductive sheet over the first surface.

32. A method according to any one of claims 20 to 31 wherein the connector interface comprises a substrate.

33. A method according to any one of claims 20 to 31 wherein the connector interface comprises an integrated circuit.

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